App Note 360: DS21352/DS21552 versus DS2152 Single Chip Transceiver

This application note will help with the migration from a current design using the DS2152 single chip transceiver (SCT) to one using the DS21352 or DS21552 SCT. These two devices are foot print compatible which allows the DS2152 to be replaced with only minor modifications to both the hardware and software. Some of the benefits of the migration to the DS21352 or DS21552 are that these devices have a more advanced HDLC, support JTAG test functions, multiple devices can communicate on a single high-speed bus, and operate at 3.3 volts with 5.0 volt tolerant I/O. To take advantage of these new functions, the application note outlines the specific hardware and software differences. It also indicates the specific sections of the DS21352 and DS21552 data sheet which have more information on the new functions what are available.

1. Introduction

This application note highlights the differences between the DS21352/DS21552 and the DS2152. The DS21352/DS21552 is a superset of the DS2152 maintaining a consistent pin out and register set. All of the original features of the DS2152 have been retained and software created for the DS2152 is transferable to the DS21352/DS21552 with minimal effort. The DS21352 and DS21552 are functionally equivalent with the only difference being the required supply voltage •Ethe DS21352 operates at 3.3V and the DS21552 operates at 5V.

2. Additional Functionality

New Features	Data Sheet Section
HDLC controller Buffer depth increased from 16 to 64 bytes HDLC over DS0 functionality added	15
JTAG	19
8 Mbps interleaved PCM bus operation	20
3.3V operation with 5V tolerant I/O (for DS21352)	23

3. Changes in Register Definitions

When implementing the new features of the DS21352/DS21552, a priority was placed on preserving the DS2152's register map to facilitate code migration from existing DS2152 designs. This section highlights register additions and differences found in the DS21352/DS21552.

3.1 New Feature Register Usage

Highlights specific registers related to new features. Each item can be found in the data sheet under the listed sections.

3.1.1 HDLC DS0 Control (section 15)

Register	Address	Description
RDC1	90h	Receive HDLC DS0 Control Register 1
RDC2	91h	Receive HDLC DS0 Control Register 2
TDC1	92h	Transmit HDLC DS0 Control Register 1
TDC2	93h	Transmit HDLC DS0 Control Register 2

3.1.2 Interleaved PCM Bus Operation (section 20)

Register	Address	Description
IBO	94h	Interleave Bus Operation

3.2 Bit Assignment Changes within Existing Registers

Highlights bit locations in the DS21352/DS21552 which have changed from the DS2152.

Register	Bit #	DS2152 Symbol	DS2152 Description	DS21352/DS21552 Symbol	DS21352/DS21552 Description
CCR3	7	ESMDM	Elastic Store Minimum Delay Mode	RESMDM	Rx Elastic Store Minimum Delay Mode
CCR3	6	ESR	Elastic Store Reset	TCLKSRC	Tx Clock Source Select
CCR3	0	N/A	Not assigned	TESMDM	Tx Elastic Store Minimum Delay Mode
CCR6	6	N/A	Not assigned	RESALGN	Rx Elastic Store Align

CCR6	5	N/A	Not assigned	TESALGN	Tx Elastic Store Align
CCR7	5	N/A	Not assigned	RESR	Rx Elastic Store Reset
CCR7	4	N/A	Not assigned	TESR	Tx Elastic Store Reset

4. Changes in Device Pin Out

4.1 Package types

The DS2152 and DS21352/DS21552 are both offered in a 100 pin 14 x 14 x 1.4mm LQFP. Values listed are for body dimensions.

4.2 Device Pin Differences

4.2.1 JTAG Pins

Pin #	DS21352/DS21552	DS2152	Description
2	JTMS	NC	IEEE 1149.1 Test Mode Select
4	JTCLK	NC	IEEE 1149.1 Test Clock Signal
5	JTRST	NC	IEEE 1149.1 Test Reset
7	JTDI	NC	IEEE 1149.1 Test Data Input
10	JTDO	NC	IEEE 1149.1 Test Data Output

4.2.2 Interleaved PCM Bus Pins

Pin #	DS21352/DS21552	DS2152	Description
36	CI	NC	Carry In
54	CO	NC	Carry Out

4.2.3 Framer Mode Select Pin

Pin #	DS21352/DS21552	DS2152	Description
76	FMS	NC	Framer Mode Select

More Information

DS21352: QuickView -- Full (PDF) Data Sheet -- Free Samples

DS2152: QuickView -- Full (PDF) Data Sheet -- Free Samples

DS21552: QuickView -- Full (PDF) Data Sheet -- Free Samples